Amendments to the Specification:

Page 1, before paragraph 1, insert:

Field of the Invention

Page 1, before paragraph 2, insert:

Description of Related Art

Page 4, paragraph No. 27, replace the existing paragraph with the paragraph below:

[27] A receiver fiber optic cable 105 carries an optical data signal to the reversed-biased photo diode 110. Photo diode 110 senses the amount of light from fiber optic cable 105 and a proportional leakage current flows from the device's cathode to anode. This current flows through sensor resistor 112, and generates a voltage. This voltage is amplified by pre-amplifier 120 and amplifier 130. Offsets are reduced by DC correction circuit 150. The DC correction circuit 150 output is fed back to the pre-amplifier 120 through resistor 136. The output of amplifier 130 drives the clock and data recovery circuit 140, as well as the link and data detect block 160. The clock and data recovery circuits extract the clock signal embedded in the data provided on line 135 by the amplifier and with it retimes the data for output on lines 143. If the link and data detect block 160 senses either a data or link signal at the data line 135, a valid signal is asserted on line 167. When the link and data detect block 160 senses a data

signal at the data line 135, a receive squelch signal is de-asserted on line 163.

Page 6 paragraph No. 34, replace the existing paragraph with the paragraph below:

[34] As its name implies, the voltage controlled oscillator is an oscillator, the frequency of which is controlled by a voltage, in this example VTUNE. As VTUNE changes, the oscillation frequency changes. If the DATA signal on lines 205 and the CLOCK signal on lines 255 do not have the desired phase relationship, the error voltage, and thus VTUNE, changes in the direction necessary to adjust the VCO in order to correct the phase error. In a specific embodiment, if the DATA signal on lines 205 comes too soon, that is, it is advanced in time relative to the clock signal on lines 255, the phase detector increases the ERROR voltage on line 222. This results in a change in the VTUNE voltage 245 that increases the frequency of the CLOCK 255. As the frequency of the CLOCK signal on lines 255 increases, its edges come sooner in time, that is they advance. This in turn, brings the clock's rising edges into alignment with transitions in the data signal on lines 205. As the edges move into alignment, the error signal on line 222 reduces, changing VTUNE 245, thereby reducing the frequency of the CLOCK signal on lines 255. <u>The retimed data 215 is output by data retiming block 210.</u> This feedback ~~insurers~~ <u>insures</u> that the DATA and CLOCK signals have the proper phase relationship for retiming the data by retiming block 210. In this condition the loop is said to be locked. Hence, these

clock and data recovery circuits are referred to as phase-locked loops.

Page 10, paragraph No. 47, replace the existing paragraph with the paragraph below:

[47] The power supplies are shown here as VDD on line [[407]] 482 and VSS on line [[417]] 471. The VDD and VSS voltages for this and all the included figures are typically equal, but are not so limited. VDD may be a positive supply above ground. For example, VDD may be 5.0, 3.3, 2.5, [[1,8]] 1.8, or other supply voltage. Alternatively, VDD may be ground. VSS may be ground. Alternately, VSS may be below ground, such as -1.8, -2.5, -3.3, -5.0, or other voltage. In other embodiments, other voltages may be used.

Page 13, paragraph No. 54, replace the existing paragraph with the paragraph below:

[54] Figure 5 is a schematic 500 of a latch with inductive broadbanding that may be used as latch 320 in Figure 3. Alternately, other types of latches may be used, for example cross coupled logic gates may be used. Included are input differential pair M1 510 and M2 515 latching pair M3 520 and M4 525, clock pair M5 550 and M6 555, current source M7 570, and series loads of inductor L1 581 and resistor R1 585, and inductor L2 538 and resistor R2 590. Data inputs DIP and DIN are received on lines 502 and 507, clock inputs CKP and CKN are received on lines 509 and 511, bias violate BIASN is received on line 579, and outputs QP (true) and QN (complementary) are

provided on lines 517 and 519. <u>Power supply VDD 582 is connected to the input differential pair M1 510 and M2 515 through inductors L1 and L2 581, 583 and resistors R1 and R2 585, 590. The other power supply VSS 571 is connected to current source M7 570.</u>

Page 14, paragraph No. 59, replace the existing paragraph with the paragraph below:

[59] Signals at the A input steer the drain currents of M16 670 through either M5 600 or M6 665. The signal at the B input steers the current to the load resistors thereby generating voltage outputs at QP and QN on lines 612 and 614. The connections are such that QP is high when the signal at either, but not both, the A input and the B input are high. To match the delay from input to output, two buffers are used in the B path, and one buffer is used in the A path. This is because the A input steers the lower devices M5 and M6, which then drive upper devices M1 through M4. But the B input drives devices M1 to M4 directly. Thus, to compensate for the delay through the M5 660 and M6 665, an extra buffer is inserted in the B path. Resistor R7 682 lowers the common mode voltage of the output of the A input buffer, <u>including M7 675 and M8 680,</u> which improves the transient response of the lower differential pair M5 660 and M6 665.

Page 21 paragraph No. 90, replace the existing paragraph with the paragraph below:

[90] Figure 13 shows this for a specific DATA

transition 1305. Shown is a timing diagram with a phase error t_9 1315 introduced between a data transition 1305 and a CLOCK rising edge 1302. Included are inputs CLOCK 1310 and DATA 1320, and resulting signals Q1 1330, Q2 1340, DLY 1350, ERROR 1360, and REFERENCE 1370. The transition 1305 in DATA 1320 results in a pulse in ERROR waveform 1370, specifically 1315, and a REFERENCE bit 1325. But this time, since the DATA 1320 has been delayed, ERROR pulse 1315 is narrower than the corresponding pulse 915 in Figure 9. Specifically, ERROR pulse 1315 is narrower by an amount shown here as to t_{10} 1317. In most cases t_{10} 1317 is approximately equal to t_9 1319. Accordingly, the average value of ERROR signal 1360 is higher than the average value of ERROR signal 960 in Figure 9. But again, since the REFERENCE pulse 1325 is defined by signals timed to the falling and rising edges of the CLOCK 1310, its width does not change as compared to REFERENCE pulse 925 in Figure 9. Therefore, the difference between the ERROR signal and the REFERENCE signal has changed, and this difference signal is used to correct for the phase error between DATA transitions such as 1305 and the rising edges of the CLOCK 1310.